

N-Channel 100V(D-S) MOSFET

GENERAL DESCRIPTION

The MEE4298-G is a N-Channel enhancement mode power field effect transistor, using Force-MOS patented Extended Trench Gate (ETG) technology. This advanced technology is especially tailored to minimize on state resistance and gate charge, and enhance avalanche capability. These devices are particularly suited for medium voltage application such as charger, adapter, notebook computer power management and other lighting dimming powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

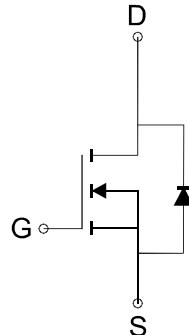
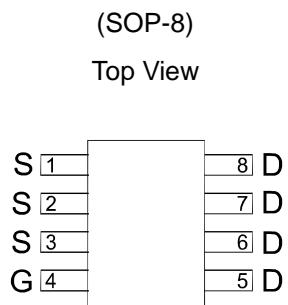
FEATURES

- $R_{DS(ON)} \leq 8\text{m}\Omega @ V_{GS}=10\text{V}$
- $R_{DS(ON)} \leq 11.5\text{m}\Omega @ V_{GS}=4.5\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- Synchronous Rectification
- Load Switch

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information:MEE4298-G (Green product- Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current*	I_D	13	A
		10.3	
Pulsed Drain Current*	I_{DM}	51.4	A
Maximum Power Dissipation*	P_D	2.8	W
		1.8	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Junction-to-Ambient Thermal Resistance*	$R_{\theta JA}$	45	$^\circ\text{C}/\text{W}$

* The device mounted on 1in² FR4 board with 2 oz copper

* Chip silicon limitation current is 100A

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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

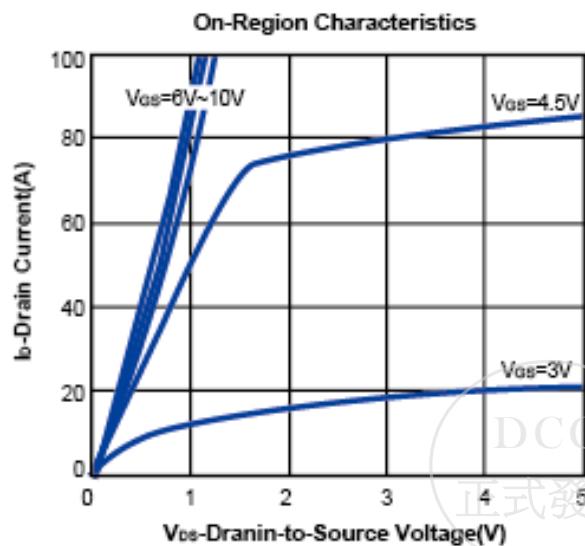
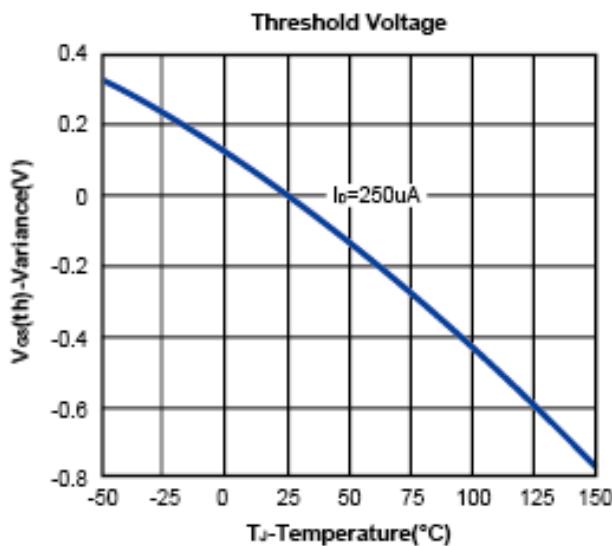
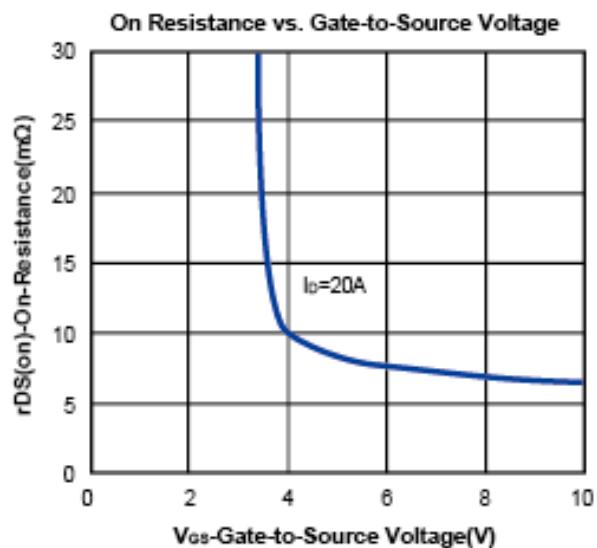
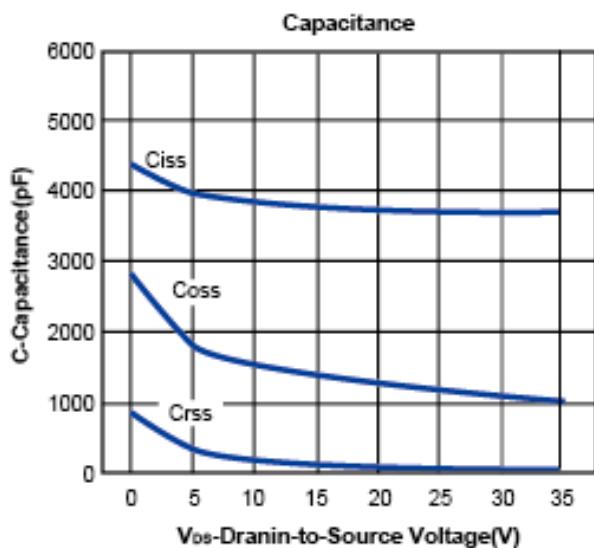
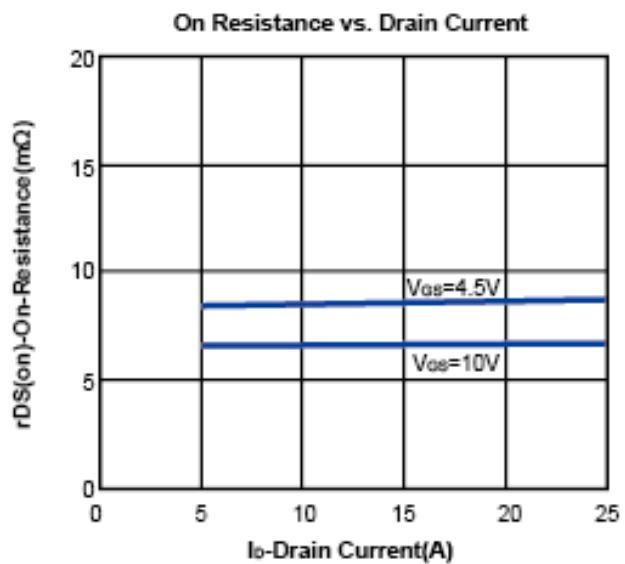
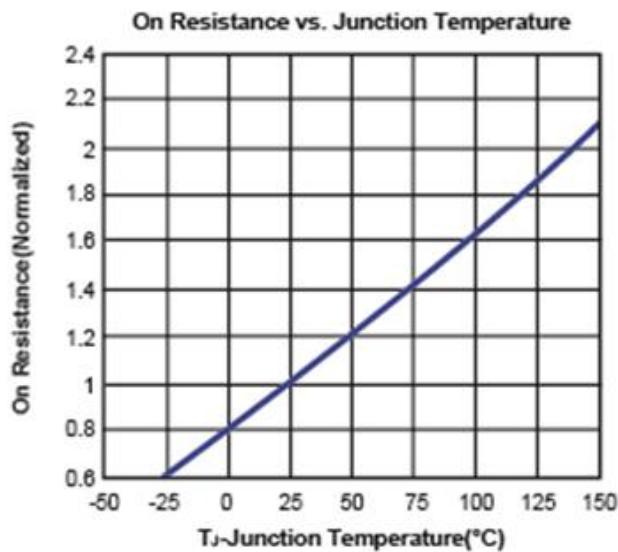
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	100			V
V _{GSS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		2.5	V
I _{GS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V			1	μA
R _{DSON}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D =11.5A		6.7	8	mΩ
		V _{GS} =4.5V, I _D =9.5A		8.8	11.5	
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V			1	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =10V, I _D =20A		66.8		nC
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =4.5V, I _D =20A		35.2		
Q _{gs}	Gate-Source Charge			12.6		
Q _{gd}	Gate-Drain Charge			14.1		
C _{iss}	Input capacitance	V _{DS} =30V, V _{GS} =0V, f=1.0MHz		3729		pF
C _{oss}	Output Capacitance			1130		
C _{rss}	Reverse Transfer Capacitance			64		
t _{d(on)}	Turn-On Delay Time	V _{DS} =50V, R _L =2.5Ω V _{GS} =10V, R _G =6Ω I _D =20A		25.4		ns
t _r	Turn-On Rise Time			46.9		
t _{d(off)}	Turn-Off Delay Time			64.3		
t _f	Turn-Off Fall Time			23.1		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

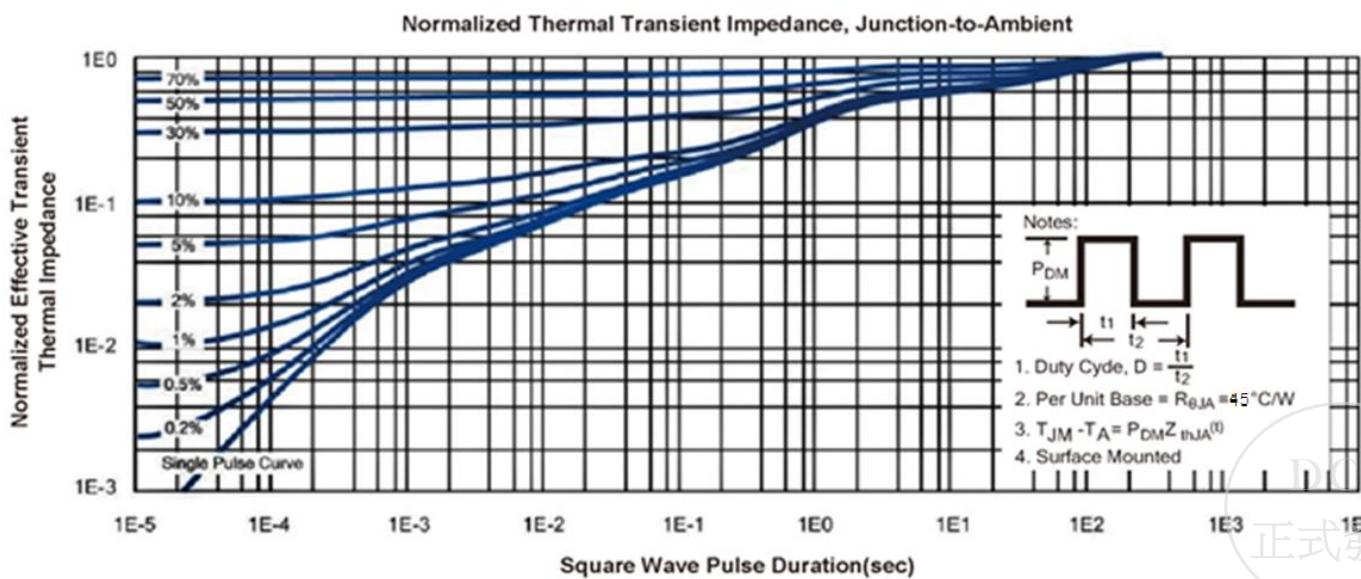
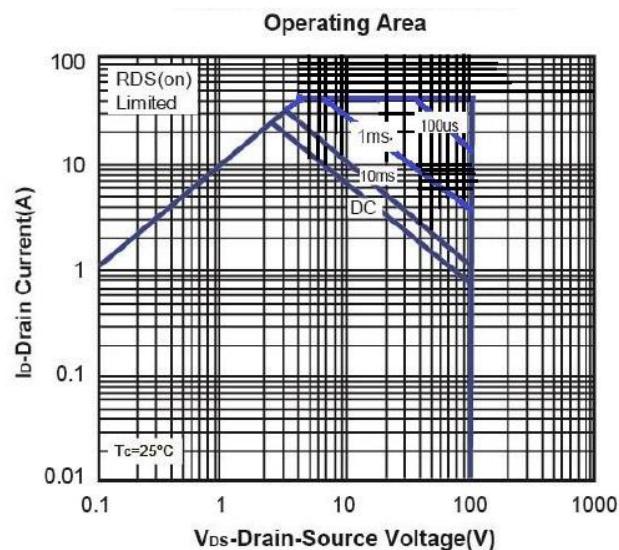
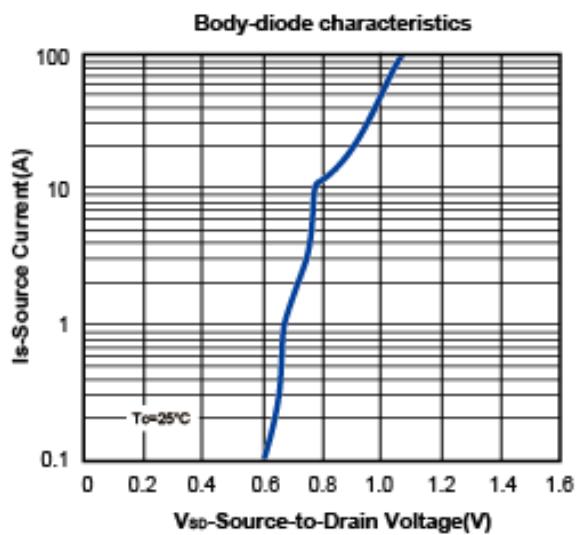
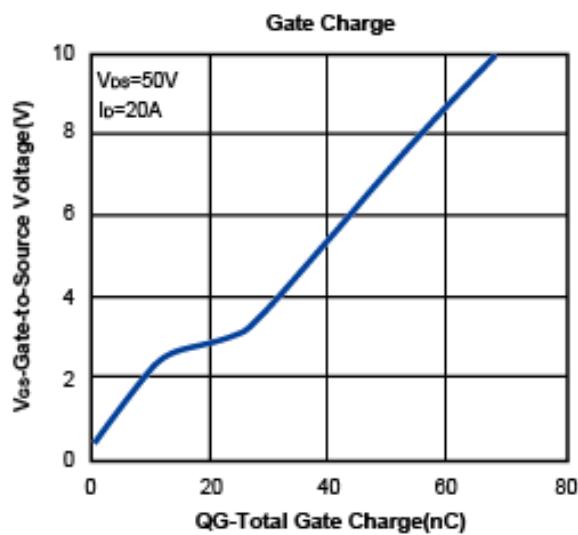
b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.



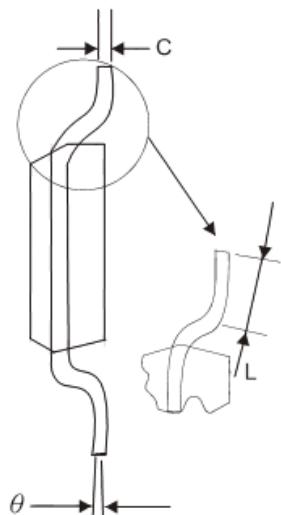
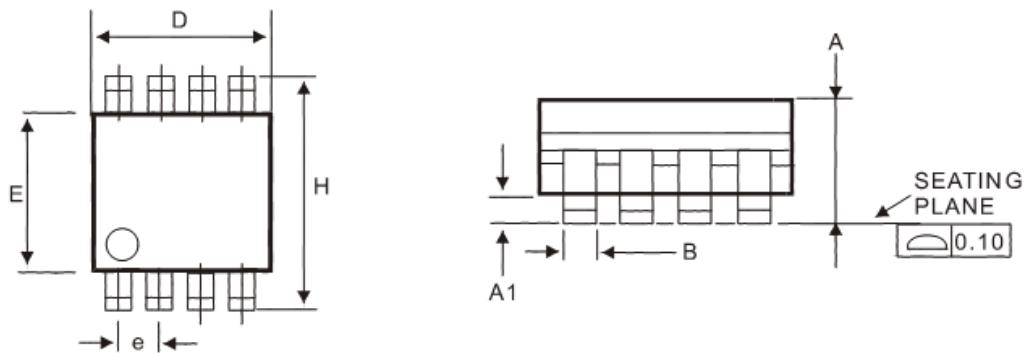
Typical Characteristics (T_J = 25°C Noted)



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 Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)


SOP-8 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.31	0.51
C	0.17	0.25
D	4.80	5.10
E	3.80	4.30
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.27
θ	0°	8°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

